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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/726.391	12/01/2000	Edward Colles Nevill	550-189	1282

7590 04/07/2004

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EXAMINER

BULLOCK JR, LEWIS ALEXANDER

ART UNIT PAPER NUMBER

2126

DATE MAILED: 04/07/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/726,391	NEVILL, EDWARD COLLES	
	Examiner	Art Unit	
	Lewis A. Bullock, Jr.	2126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 December 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Request for Reference Cited in the Specification

On page 9, lines 10-12 of the specification, Applicant identifies that a detailed description of this may be found in "The Java Virtual Machine Specification" (Edition 1) by Tim Lindholm and Frank Yellin published by Addison Wesley, ISBN 0-201-63452-X. The examiner request Applicant to furnish the cited reference to be considered for the application.

Drawings

1. New corrected drawings are required in this application because of Draftpersons' Review. Applicant is advised to employ the services of a competent patent draftsman outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

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only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 7-14 are rejected under 35 U.S.C. 102(e) as being anticipated by BAK (US 6,513,156).

As to claim 1, BAK teaches an apparatus (computer system) for processing data, the apparatus comprising: a processor core (central processor); a main memory (system memory) operable to store instruction words and data words (col. 4, line 58 – col. 5, line 20); a data store (bytecode table) operable to store words from the main memory accessed by a data store port of the processor core (col. 12, lines 53 – col. 13, line 30); an instruction store (snippet zone / template table) operable to store words from the main memory accessed by an instruction store port of the processor core (col. 8, lines 11-42; col. 12, lines 53 – col. 13, line 30); and an instruction interpreter (interpreter / virtual machine) operable to read instruction words from the instruction store (col. 5, lines 31-61; col. 6, line 61 – col. 7, line 11); wherein the instruction interpreter (interpreter / virtual machine) is operable to modify a slow form instruction (original virtual machine instruction) within the instruction store to a fast form instruction (new virtual machine instruction) and to write the fast form instruction to the data store (via overwriting the original virtual machine instruction with the new virtual machine instruction) (col. 7, lines 12-67; col. 9, lines 6-62), the slow form instruction and the fast form instruction having a common functionality when executed by the interpreter (executes the same function); and the instruction interpreter (interpreter / virtual machine) is operable upon reading a slow form instruction (original virtual machine instruction) from the instruction store to check for a corresponding fast form instruction

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(new virtual machine instruction) within the data store and if the fast form instruction is present within the data store, then to execute the fast form instruction instead of the slow form instruction (col. 7, lines 12-67; col. 8, lines 1-58).

As to claim 7, BAK teaches the slow form instruction results in an unresolved storage access request to one or more stored words (via the amount of execution time to load the values or next instruction for execution) and the fast form instruction results in a resolved storage access request to the one or more stored words (via referencing the information already stored) (col. 6, lines 5-50).

As to claim 8, BAK teaches the slow form instruction (original virtual machine instructions) includes a symbolic reference to a required element (loop instructions) (col. 8, line 59 – col. 9, line 5) and the fast form instruction (new virtual machine instruction) includes a numeric reference to the required element (index to snippet) (col. 8, lines 11-26, lines 43-58).

As to claim 9, BAK teaches the slow form instruction (typical java bytecodes) invokes an additional data processing procedure before completion (compilation into bytecodes and then being interpreted) (col. 5, lines 13-20).

As to claim 10, BAK teaches the slow form instruction and the fast form instructions are Java Virtual Machine Instructions (col. 5, lines 13-20; col. 7, lines 28-53).

As to claim 11, BAK teaches the slow form instructions are getstatic, putstatic or invoke (col. 8, line 59 – col. 9, line 5).

As to claim 12, BAK teaches the fast form instruction is invokenonvirtual_quick (go-native instruction) (col. 8, lines 1-58).

As to claim 13, BAK teaches the instruction interpreter (interpreter / virtual machine) translates Java Virtual Machine instructions to native instructions of the processor core (col. 6, line 31 – col. 7, line 67).

As to claim 14, reference is made to a method that corresponds to the apparatus of claim 1 and is therefore met by the rejection of claim 1 above.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 2-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over BAK (US 6,513,156).

As to claims 2-4, BAK teaches an instruction interpreter for translating and interpreting the instructions (col. 5, lines 31-61; col. 6, line 61 – col. 7, line 11).

However, BAK, does not mention whether the interpreter is hardware-based, software-based, or a combination of both. Official Notice is taken in that it is well known in the art that an interpreter is implemented as a hardware interpreter, a software interpreter, or a combination of both and therefore would be obvious to one skilled in the art that the interpreter is one of a software interpreter, a hardware interpreter, or a combination of both in order to interpret the instructions.

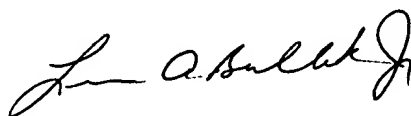
As to claims 5-6, BAK teaches the data store and instruction store is used by the system in determining whether there exist and to use a fast form instruction (new virtual machine instruction) (col. 12, lines 53 – col. 13, line 30; col. 7, lines 12-67; col. 8, lines 1-58; col. 9, lines 6-62). It is inherent within the teachings that the stores reside in system memory. BAK also teaches that the computer system includes more than one processor or a cache memory (col. 5, lines 1-2). However, BAK does not teach that the stores are maintained in a data cache. Official Notice is taken in that it is well known to one of ordinary skill in the art that the stores may reside on the cache for quick access.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lewis A. Bullock, Jr. whose telephone number is (703) 305-0439. The examiner can normally be reached on Monday-Friday, 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (703) 305-9678. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read "Lewis A. Bullock, Jr.", is positioned in the lower right area of the page.

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